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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/943,078	08/30/2001	Todd R. Abbott	MIO 0083 PA	7688

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EXAMINER	
KIELIN, ERIK J	

ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 04/12/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/943,078	ABBOTT, TODD R.	
	Examiner	Art Unit	
	Erik Kielin	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 November 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *50-58* is/are pending in the application.

4a) Of the above claim(s) *none* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *50-58* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2/2/5*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 8 November 2004 has been entered.

Election/Restrictions

2. Newly submitted claims 53 and 54 are directed to an invention that is independent or distinct from the invention originally claimed for the following reasons: New claims 53 and 54 are not drawn to the elected species IA of the restriction requirement of 9/20/2002. Applicant indicates that claims 53 and 54 do not read on the elected species in the Response filed 2/2/2005.

Since applicant has received an action on the merits for the originally presented invention, this invention has been constructively elected by original presentation for prosecution on the merits. Accordingly, claims 53 and 54 are withdrawn from consideration as being directed to a non-elected invention. See 37 CFR 1.142(b) and MPEP § 821.03.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claims 50-58 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The instant specification fails to provide support for the limitations, that the lightly-doped drain regions and source/drain regions are "adjacent and lateral to local interconnect structure." This is not discussed in the specification or shown in the drawings. Accordingly this is new matter.

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claim 58 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

7. Claim 58 recites the limitation "**said damascene local interconnect structure**" in lines 15-16. There is insufficient antecedent basis for this limitation in the claim. The local interconnect structure has not yet been formed at this point. It is assumed that the local interconnect structure is formed during the filling of the damascene trench followed by planarization. For the purposes of patentability, the claims will be interpreted as best understood.

8. Claim 58 recites the limitation, "forming doped source/drain regions in said base substrate after forming said spacers such that said base substrate is doped more deeply into said base substrate **adjacent and lateral to** said spacers than into said base substrate underneath said

spacers." The phrase in bold is entirely unclear. The light-doped drain regions are beneath the spacers, not the source/drain regions.

Claim Rejections - 35 USC § 102

9. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

10. Claims 50-52 are rejected under 35 U.S.C. 102(b) as being anticipated by US 6,083,827 (**Lin** et al.).

Regarding claim 50, **Lin** discloses a method of fabricating a semiconductor device comprising:

forming a damascene trench **232** in a first dielectric layer **218**, **228** over a base substrate **200**, said damascene trench having a gate area and a local interconnect are (Fig. 2C);

depositing a conductive layer **238**, **240** over said base substrate **200** such that said damascene trench is filled with a conductive material **238**, **240** (Fig. 2D);

planarizing said device to define a damascene structure including a damascene gate structure and a damascene local interconnect structure electrically coupled by said conductive material within said damascene trench, wherein said damascene local interconnect structure **238**, **240** forms a direct connection to said base substrate **200** (Fig. 2E);

providing at least one implant contact **226** within a plug area, wherein said plug area is located at least partially beneath and in contact with said damascene local interconnect structure (Fig. 2E);

and forming doped source/drain regions **226** in said base substrate **200** adjacent and lateral to said damascene gate structure and said damascene local interconnect structure.

Regarding claim 51, the method of fabricating a semiconductor device of claim 50, further comprising:

forming an isolation trench **202** in said base substrate before said first dielectric layer **218**, **228** is formed (Fig. 2E).

Regarding claim 52, the method of fabricating a semiconductor device of claim 51, wherein at least a portion of said damascene trench **232** partially overlies said isolation trench **202** (Fig. 2E).

Claim Rejections - 35 USC § 103

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

12. Claims **58** is rejected under 35 U.S.C. 103(a) as being unpatentable over **Tsutsumi** in view of the basic text of **Ghandi**, VLSI Fabrication Principles, 2nd ed., John Wiley & Sons: New York, 1994, pp. 452, 456, and considered with Van Zant, Microchip Fabrication, 4th ed. McGraw-Hill: New York, 2000, p. 199 for a showing of inherency only.

Tsutsumi discloses a method of fabricating a semiconductor device comprising:

forming an isolation region **2** in a base substrate **1**;

forming a first dielectric layer **3** over said base substrate **1**;

forming a first patterned mask over said first dielectric layer (Fig. 2);

etching through said first dielectric layer to said base substrate in areas defined by said first patterned mask to define a damascene trench in said first dielectric layer, said damascene trench having a gate area and a local interconnect area and positioned such that at least a portion of said damascene trench at least partially overlies said isolation trench (Fig. 2; paragraph bridging cols. 13-14; Figs. 45, 48, 50, 51, 54, 55, 60, 65);

stripping said first patterned mask from said first dielectric layer **3** (Fig. 2; see **NOTE** below regarding inherency);

growing an oxide layer **36** on said base substrate, said oxide layer **36** within said gate area of said damascene trench defining a gate oxide layer (Figs. 7, 68);

forming a second patterned mask **33**, **34** over said semiconductor device, said second patterned mask **33**, **34** arranged to expose at least a portion of said oxide layer **36** within said local interconnect area, wherein said damascene local interconnect structure forms a direct connection to said base substrate;

etching away the exposed portion of said oxide layer **36** within said damascene trench **4**;

providing at least one contact implant **5b**, **11**, **13**, **21** within said base substrate **1** through said damascene trench (Figs. 2, 10, 11, 23);

stripping said second patterned mask from said semiconductor device (Fig. 68; see also Figs. 58-70 and col. 25, line 1 to col. 26, line 20);

depositing a conductive layer **10**, **14**, **32** comprising a conductive material over said device such that said conductive layer fills said damascene trench **4** (Figs. 13, 68);

planarizing said conductive layer down to the surface of said dielectric layer to said gate and local interconnect areas, wherein said damascene local interconnect structure forms a direct connection to said base substrate (Figs. 13, 14);

removing said first dielectric layer to define a damascene gate structure and a damascene local interconnect structure **3**, **33**, **34** (Figs. 45, 48, 50, 51, 54, 55, 60, 65);

forming lightly doped drain regions **11** in said base substrate **1** adjacent to said damascene gate structure **10** and said damascene local interconnect structure **10**, **14**, **32**;

depositing a spacer layer **12** over said device;

anisotropically etching said spacer layer such that spacers are formed over the portions of said base substrate where said lightly doped drain regions are formed (Figs. 15-17); and

forming doped source/drain regions **13** in said base substrate **1** after forming said spacers **12** such that said base substrate is doped more deeply into said base substrate adjacent and lateral to said spacers than into said base substrate underneath said spacers.

NOTE: **Tsutsumi** discloses that the damascene trench is formed by "photolithography and etching" (paragraph bridging cols. 13-14), which inherently comprises,

forming a patterned mask over said first dielectric layer;

etching through said first dielectric layer to said base substrate in areas defined by said patterned mask; and

stripping said patterned mask from said first dielectric layer.

(See Van Zant, Microchip Fabrication, 4th ed. McGraw-Hill: New York, 2000, p. 199 for verification.)

Tsutsumi does not state that the oxide isolation film **2** is a "trench" formed "in" the base substrate **1**.

Ghandi teaches that thermal oxidation of the silicon substrate to form SiO_2 reduces leakage current by reducing surface state density (p. 452, section entitled "7.1 Thermal Oxidation of Silicon") is better than deposition for forming oxides on a semiconductor substrate to prevent leakage current generated by dangling bonds at the interface. **Ghandi** also teaches that oxidation consumes the silicon substrate in which it is formed, accordingly the isolation trench is formed "in" the substrate by thermal oxidation (p. 456, section entitled "7.1.3 Oxide formation").

It would have been obvious for one of ordinary skill in the art, at the time of the invention to use thermal oxidation of the base substrate **1** of **Tsutsumi** to form the isolation trench **2**, in order to reduce leakage current, as taught by **Ghandi**. Moreover, because **Tsutsumi** is silent to the method by which the isolation trench 2 is formed, one of ordinary skill would be motivated to use the well known method taught in **Ghandi** to reduce time in research developing a new method.

13. Claims 55-57 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Tsutsumi** in view of **Lin**.

Regarding claim 55, in addition to all of the features above, **Tsutsumi** discloses that the conductive material used to form the gate and local interconnect area comprises polysilicon and

that a metal silicide may be formed over the polysilicon (Tsutsumi, col. 17, lines 14-22; col. 18, first paragraph).

Regarding claims 56 and 57, in addition to all of the features above, **Tsutsumi** discloses the formation of lightly-doped drain regions **11** after removing the first dielectric layer **2**, **3** and also forms spacers 12 against the vertical walls of said damascene gate structure and said local interconnect structure (Figs. 9-11).

As applied to each of the claims 55-57, **Tsutsumi** does not indicate that the local interconnect structure and the gate structure are electrically coupled by the conductive material in the damascene trench.

Lin teaches integration of the formation of the gate structure and local interconnect wherein the local interconnect structure and the gate structure are electrically coupled by the conductive material in the damascene trench.

It would have been obvious for one of ordinary skill in the art, at the time of the invention to have the local interconnect structure and the gate structure electrically coupled by the conductive material in the damascene trench in **Tsutsumi**, in order to integrate the formation of the local interconnect structure and the gate structure, which save time, as taught by **Lin**.

Response to Arguments

14. Applicant's arguments with respect to claims 50-58 have been considered but are moot in view of the new ground(s) of rejection.

Applicant argues that Tsutsumi fails to disclose that the source/drain regions are adjacent and lateral to the local interconnect. So does the instant disclosure. This is new matter and is therefore not persuasive of novelty.

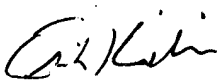
Applicant additionally argues that Tsutsumi fails to show a direct connection to the base substrate and that there is no contact implant. Applicant is exceedingly mistaken, as these features are shown in numerous figures, as noted in the rejections above.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Erik Kielin whose telephone number is 571-272-1693. The examiner can normally be reached from 9:00 - 19:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr. can be reached on 571-272-1702. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Erik Kielin
Primary Examiner
April 9, 2005